## Asynchronous Parallel DLA in Concurrent Collections

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#### Motivation and goals

Motivating recent work for multicore systems

- Tile algorithms for DLA, *e.g.*, Buttari, *et al*. (2007); Chan, *et al*. (2007)
- General parallel programming models suited to this algorithmic style, e.g., Concurrent Collections (CnC) by Knobe & Offner (2004)

#### Goals

- Study: Apply and evaluate CnC using PDLA examples
- Talk: CnC tutorial crash course; platform for your work?

### Outline

- Overview of the Concurrent Collections (CnC) language
- Asynchronous parallel Cholesky & symmetric eigensolver in CnC
- Experimental results (preliminary)

# Concurrent Collections (CnC) programming model

- Separates computation semantics from expression of parallelism
- Program = components + scheduling constraints
- Components: Computation, control, data
- Constraints: Relations among components
- No overwriting of data, no arbitrary serialization, and no side-effects
- Combines tuple-space, streaming, and dataflow models

 $Z \leftarrow x \cdot y^T$ 

$$Z \leftarrow x \cdot y^T$$
$$z_{i,j} \leftarrow x_i \cdot y_j$$

Example only; coarser grain may be more realistic in practice.

 $z_{i,j} \leftarrow x_i \cdot y_j$ 

**Collections:** Static representation of dynamic *instances* 

 $z_{i,j} \leftarrow x_i \cdot y_j$ 

#### **Collections:**

Static representation of dynamic *instances* 



Unit of execution



Set of all (dynamic) multiplications



#### $\langle a, b, \ldots \rangle$ = tuple of tag components



#### Says *whether*, not *when*, step executes 10



#### Tags **prescribe** steps







#### "Environment" may produce/consume

## Essential properties of a CnC program

- Written in terms of values, without overwriting ⇒ race-free (dynamic single assignment)
- No arbitrary serialization, only explicit ordering constraints (avoids analysis)
  - Steps are side-effect free (functional)





match ← find (value x in tree T)





match ← find (value x in tree T)













▶ Tag <i=2, j=5> available
 ⇒ Step prescribed

 $z_{i,j} \leftarrow x_i \cdot y_j$ 



- ► Tag <2,5> available
   ⇒ Step prescribed
- ▶ Items x:<2>, y:<5> available
   ⇒ Step *inputs-available*

 $z_{i,j} \leftarrow x_i \cdot y_j$ 



- Tag <2,5> available
   ⇒ Step prescribed
- ▶ Items x:<2>, y:<5> available
   ⇒ Step inputs-available

Prescribed + inputs-available
 ⇒ enabled

- $z_{i,j} \leftarrow x_i \cdot y_j$ <2>
  <2>
  ×
  <2>
  ×
  <2,5>
  ×
  <2,5>
  ×
  <2,5>
  ×
  <2,5>
  ×
  <2,5>
  ×
  <2,5>
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- Tag <2,5> available
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   ⇒ Step inputs-available

Prescribed + inputs-available
 ⇒ enabled

Executes ⇒ Z:<2,5> *available* 

## Coding and execution

- [1] Write the specification (graph).
- [2] Implement steps in a "base" language (C/C++).
- [3] Build using CnC translator + compiler.

[4] Run-time system maintains collections and schedules step execution.















// Input:

env  $\rightarrow$  <\*: i,j>;



// Input:

env → <\*: i,j>, [x: i], [y: j];



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env → <\*: i,j>, [x: i], [y: j];
// Prescription relations:

<\*: i,j> :: (\*: i,j);

 $z_{i,j} \leftarrow x_i \cdot y_j$ 



// Input: env → <\*: i,j>, [x: i], [y: j]; // Prescription relations: <\*: i,j> :: (\*: i,j); // Producer/consumer relations: [x: i], [y: j] → (\*: i, j); (\*: i, j) → [Z: i, j];

 $z_{i,j} \leftarrow x_i \cdot y_j$ 

// Input: env → <\*: i,j>, [x: i], [y: j]; // Prescription relations: <\*: i,j> :: (\*: i,j); // Producer/consumer relations: [x: i], [y: j] → (\*: i, j); (\*: i, j) → [Z: i, j]; // Output:  $[Z: i, j] \rightarrow env;$ 

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// Input: env → <\*: i,j>, [x: i], [y: j]; // Prescription relations: <\*: i,j> :: (\*: i,j); // Producer/consumer relations: [x: i], [y: j] → (\*: i, j);  $(*: i, j) \rightarrow [Z: i, j];$ // Output:  $[Z: i, j] \rightarrow env;$ 

 $z_{i,j} \leftarrow x_i \cdot y_j$ 



Return\_t mult (Graph\_t& G,

const Tag\_t& t)

{
 int i = t[0], j = t[1];
 double x\_i = G.x.Get (Tag\_t(i));
 double y\_j = G.y.Get (Tag\_t(j));
 G.Z.Put (Tag\_t(i, j), x\_i\*y\_j);
 return CNC\_Success;

Intel's implementation uses C++; Rice University's uses Java (Habanero)

}

{

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#### Run-time system

Built on top of Intel Threading Building Blocks (TBB)

Implements Cilk-style work stealing scheduler

- Work queues use LIFO, but FIFO and other strategies in development
- Other run-times possible
- DEC/HP TStreams on MPI; Rice U. Habanero uses Java threads
- Intel-specific issues with queuing (more later)



Iteration k: // Over diagonal tiles

SeqCholesky ( $L_{k,k} \leftarrow A_{k,k}$ )

Trisolve  $(L_{k+1:p,k} \leftarrow A_{k+1:p,k}, L_{k,k})$ 

Update  $(A_{k+1:p,k+1:p} \leftarrow L_{k+1:p,k}, A_{k+1:p,k+1:p})$ 



Iteration k: // Over diagonal tiles SeqCholesky ( $L_{k,k} \leftarrow A_{k,k}$ ) Trisolve ( $L_{k+1:p,k} \leftarrow A_{k+1:p,k}, L_{k,k}$ ) Update ( $A_{k+1:p,k+1:p} \leftarrow L_{k+1:p,k}, A_{k+1:p,k+1:p}$ )



Iteration *k*: // Over diagonal tiles SeqCholesky ( $L_{k,k} \leftarrow A_{k,k}$ ) **Trisolve (L\_{k+1:p,k} \leftarrow A\_{k+1:p,k}, L\_{k,k})** Update ( $A_{k+1:p,k+1:p} \leftarrow L_{k+1:p,k}, A_{k+1:p,k+1:p}$ )



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## Tile Cholesky in CnC



SeqCholesky ( $L_{k,k} \leftarrow A_{k,k}$ )

Trisolve ( $L_{k+1:p,k} \leftarrow A_{k+1:p,k}$ ,  $L_{k,k}$ )

Update  $(\overline{A_{k+1:p,k+1:p}} \leftarrow L_{k+1:p,k}, \overline{A_{k+1:p,k+1:p}})$ 



Omitted: Items







Given k, multiple T steps could go  $\Rightarrow$  2-D tag





Sequential Cholesky step enables Trisolve steps





Similarly, Trisolve step enables Update steps



Other arrangements possible, *e.g.*, pre-generate all tags.

# Dense symmetric generalized eigensolver

- "Straightforward" translation of LAPACK's  $\_sygvx$  for  $Az = \lambda Bz$
- Pieces: Cholesky / reduction to standard form; tridiag reduction
- Only partly "asynchronous," but useful proof-of-concept
- Performance limited by tridiagonal reduction step (BLAS-2)

### Experimental results



**Cholesky performance:** 

Intel 2-socket x 4-core Harpertown @ 2 GHz + Intel MKL 10.1



Normalized Execution Time

CnC-based Cholesky timeline (n=1000):

Intel 2-socket x 4-core Harpertown @ 2 GHz + Intel MKL 10.1 for sequential components



Cholesky performance: AMD 4-socket x 4-core Barcelona @ 2 GHz



AMD Barcelona (4x4 = 16 core)

#### Summary and future work

#### CnC's key ideas

- Decompose computation into steps + (data) items + (control) tags, with constraint relations among these components dataflow-like
- Goal: Separate computation semantics (orderings) from parallelism
- Ongoing
  - Finish" proof-of-concept example by adding, *e.g.*, blocked data layouts
  - New language primitives to simplify tag management & improve modularity, performance
  - Extending run-time scheduling infrastructure
  - Other applications & architectures

### Additional limitations

- Tag types: integers only
- Cannot handle continuous (streaming) input
- More natural support for in-place algorithms
- Tools, *e.g.*, debugging