Towards a multifrontal QR factorization for heterogeneous architectures over runtime systems

Preliminary work on multicore architectures

Florent Lopez, Joint work with IRIT Toulouse, LaBRI / Inria Bordeaux, LIP / Inria

Lyon

MUMPS Users Group Meeting, May 29-30, 2013
Context of the work
The multifrontal QR factorization is guided by a graph called an *elimination tree*:

- at each node of the tree $k$ pivots are eliminated
- each node of the tree is associated with a relatively small dense matrix called a *frontal matrix* (or, simply, a *front*) which contains the $k$ columns related to the pivots and all the other coefficients concerned by their elimination

\[
\begin{array}{ccccccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 \\
1 & a & a & a & . & . & . & . & . \\
2 & a & a & a & . & . & . & . & . \\
3 & a & a & a & . & . & . & . & . \\
4 & a & a & a & . & . & . & . & . \\
5 & a & a & a & . & . & . & . & . \\
6 & a & a & a & . & . & . & . & . \\
7 & a & a & a & . & . & . & . & . \\
8 & a & a & a & . & . & . & . & . \\
9 & a & a & a & . & . & . & . & . \\
\end{array}
\]
Accelerated architectures including GPUs are extremely popular in the HPC community:

- high density of computational units clocked at low frequencies (wrt the latest generation of CPUs)
  - high potential performance peak for parallel applications
  - limited power consumption

New generation of accelerators: MIC (Many Integrated Core) architecture

- 60 cores (In-order core derived from Pentium: energy efficient)
- clocked at 1053 MHz
- 240 threads (with 4 hyper threading sibling per core)
- advanced VPU per core (512-bit SIMD)

Incompatible programming models ⇒ specific kernels and algorithms to achieve performance
Accelerated architectures (ACC: GPU or MIC)

- an extremely heterogeneous workload
- a heterogeneous architecture
- mapping tasks is challenging
Accelerated architectures (ACC: GPU or MIC)

- management of data consistency by hand
- architecture dependant approach
- difficult to maintain

Elimination tree

Heterogeneous platform
Another option is to exploit the features of a modern runtime system capable of handling the scheduling and the data consistency in a dynamic way.
Runtime system: abstract layer between application and machine with the following features:

- automatic detection of the **task dependencies**

- dynamic task **scheduling** on different types of processing units.

- management of **multi-versioned** tasks (an implementation for each type of processing unit)

- **consistency management** of manipulated data.
Objective of the study: evaluate the usability and the effectiveness of a general purpose runtime system with complex and irregular workload such as a sparse factorization.

- exploitation of GPU-accelerated architectures

This approach is widely adopted in the case of dense linear algebra:

- PLASMA (QUARK)
- DPLASMA (PaRSEC)
- MAGMA-MORSE (StarPU)
- FLAME (SuperMatrix)

It is challenging for complex and irregular problems such as sparse linear algebra (related work on PaStiX with Pierre Ramet).
Multifrontal QR factorization on multicore over StarPU
parallelism and scheduling strategy in \texttt{qr\_mumps}

In \texttt{qr\_mumps} node and tree parallelism are exploited consistently, by partitioning the frontal matrices and replacing the elimination tree with a DAG:

the scheduler efficiency is constrained by the tasks search-space: the scheduling complexity depends on the number of active fronts and therefore is not very scalable.
In **qr_mumps** node and tree parallelism are exploited consistently, by partitioning the frontal matrices and replacing the elimination tree with a DAG:

the scheduler efficiency is constrained by the **tasks search-space**: the **scheduling complexity** depends on the number of active fronts and therefore is not very scalable. Replace the ad hoc scheduler in **qr_mumps** with a general purpose runtime system
• Depending on the input/output, StarPU detects the dependencies among tasks
• Depending on the availability of resources and the data placement, StarPU decides where to run a task
Original sequence:
1: \textit{fun}_1(A: \text{inout}, B: \text{in})
2: \textit{fun}_2(A: \text{inout})
3: \textit{fun}_1(C: \text{inout}, D: \text{in})

Equivalent StarPU code:
1: \texttt{submit\_task(}\textit{fun}_1, A: \text{inout}, B: \text{in}, \textit{id} = \textit{id}_1)\
2: \texttt{submit\_task(}\textit{fun}_2, A: \text{inout}, \textit{id} = \textit{id}_2)\
3: \texttt{declare\_dependency(}\textit{id}_3 \leftarrow \textit{id}_1)\
4: \texttt{submit\_task(}\textit{fun}_1, C: \text{inout}, D: \text{in}, \textit{id} = \textit{id}_3)

\begin{tikzpicture}
  \node (id1) at (0,0) {id$_1$};
  \node (id2) at (2,1) {id$_2$};
  \node (id3) at (2,-1) {id$_3$};
  \draw [->] (id1) to [bend right=30] (id2);
  \draw [->] (id1) to [bend left=30] (id3);
  \draw [dotted] (id2) to (id3);
  \node at (2.5,0) {\textit{detected dependency}};
  \node at (2.5,0.5) {(data hazard)};
  \node at (2.5,-0.5) {\textit{explicit dependency}};
\end{tikzpicture}
The multifrontal QR factorization: StarPU integration

Original sequence:
1: $fun_1(A: \text{inout}, B: \text{in})$
2: $fun_2(A: \text{inout})$
3: $fun_1(C: \text{inout}, D: \text{in})$

Equivalent StarPU code:
1: `submit_task(fun_1, A: \text{inout}, B: \text{in}, id = id_1)`

**detected dependency (data hazard)**

**explicit dependency**
The multifrontal QR factorization: StarPU integration

Original sequence:
1: \( \text{fun}_1(A: \text{inout}, B: \text{in}) \)
2: \( \text{fun}_2(A: \text{inout}) \)
3: \( \text{fun}_1(C: \text{inout}, D: \text{in}) \)

Equivalent StarPU code:
1: \( \text{submit}_\text{task}(\text{fun}_1, A: \text{inout}, B: \text{in}, id = id_1) \)
2: \( \text{submit}_\text{task}(\text{fun}_2, A: \text{inout}, id = id_2) \)

\( id_1 \) detected dependency (data hazard)
\( id_2 \) explicit dependency
The multifrontal QR factorization: StarPU integration

Original sequence:

1: \( \text{fun}_1(A: \text{inout}, B: \text{in}) \)
2: \( \text{fun}_2(A: \text{inout}) \)
3: \( \text{fun}_1(C: \text{inout}, D: \text{in}) \)

Equivalent StarPU code:

1: \( \text{submit\_task(} \text{fun}_1, A: \text{inout}, B: \text{in}, id = id_1) \)
2: \( \text{submit\_task(} \text{fun}_2, A: \text{inout}, id = id_2) \)

\( id_1 \) detected dependency (data hazard)

\( id_1 \) \( id_2 \) detected dependency

\( id_1 \) \( id_2 \) explicit dependency
The multifrontal QR factorization: StarPU integration

Original sequence:
1: \textit{fun}_1(A: \text{inout}, B: \text{in})
2: \textit{fun}_2(A: \text{inout})
3: \textit{fun}_1(C: \text{inout}, D: \text{in})

Equivalent StarPU code:
1: \texttt{submit\_task}(\textit{fun}_1, A: \text{inout}, B: \text{in}, \textit{id} = \textit{id}_1)
2: \texttt{submit\_task}(\textit{fun}_2, A: \text{inout}, \textit{id} = \textit{id}_2)
3: \texttt{declare\_dependency}(\textit{id}_3 \text{ id}_1)
4: \texttt{submit\_task}(\textit{fun}_1, C: \text{inout}, D: \text{in}, \textit{id} = \textit{id}_3)

\begin{itemize}
  \item detected dependency (data hazard)
  \item explicit dependency
\end{itemize}
The multifrontal QR factorization: StarPU integration

Original sequence:
1: \textit{fun}_1(A: inout, B: in)
2: \textit{fun}_2(A: inout)
3: \textit{fun}_1(C: inout, D: in)

Equivalent StarPU code:
1: \textit{submit\_task}(\textit{fun}_1, A: inout, B: in, id = id_1)
2: \textit{submit\_task}(\textit{fun}_2, A: inout, id = id_2)
3: \textit{declare\_dependency}(id_3 \leftarrow id_1)
4: \textit{submit\_task}(\textit{fun}_1, C: inout, D: in, id = id_3)

---

**detected dependency (data hazard)**

**explicit dependency**
The easy way: replace all the
call \texttt{operation1}(i1, ..., in, o1, ..., om)
with
call \texttt{submit\_task}(operation1, i1, ..., in, o1, ..., om)
and let StarPU do all the work
The multifrontal QR factorization: StarPU integration

- the DAG may have millions of nodes which makes the scheduling job too complex and memory consuming
- the scheduling of activation tasks have to be controlled in order to limit the memory consumption
Our approach: We give to StarPU a limited view of the DAG; this is achieved by defining tasks that submit other tasks.
The activation tasks in charge of allocating the memory and preparing the data structures needed for processing a front are the ideal candidates to submit the numerical tasks.
The multifrontal QR factorization: dynamic construction of the DAG

- all the activation tasks are submitted at once with explicit dependencies and a very low priority; this is done in order to prevent StarPU from executing all the activations first.

- Upon activation, the numerical tasks corresponding to the activated front are submitted with higher priorities depending on their position in the DAG.

- The DAG is progressively unrolled during the factorization and therefore the DAG size is limited as well as the memory consumption.
all the activation tasks are submitted at once with explicit dependencies and a very low priority; this is done in order to prevent StarPU from executing all the activations first.

Upon activation, the numerical tasks corresponding to the activated front are submitted with higher priorities depending on their position in the DAG.

The DAG is progressively unrolled during the factorization and therefore the DAG size is limited as well as the memory consumption.
all the activation tasks are submitted at once with explicit dependencies and a very low priority; this is done in order to prevent StarPU from executing all the activations first.

Upon activation, the numerical tasks corresponding to the activated front are submitted with higher priorities depending on their position in the DAG.

The DAG is progressively unrolled during the factorization and therefore the DAG size is limited as well as the memory consumption.
all the activation tasks are submitted at once with explicit dependencies and a very low priority; this is done in order to prevent StarPU from executing all the activations first

Upon activation, the numerical tasks corresponding to the activated front are submitted with higher priorities depending on their position in the DAG

The DAG is progressively unrolled during the factorization and therefore the DAG size is limited as well as the memory consumption
• all the activation tasks are submitted at once with explicit dependencies and a very low priority; this is done in order to prevent StarPU from executing all the activations first
• Upon activation, the numerical tasks corresponding to the activated front are submitted with higher priorities depending on their position in the DAG
• The DAG is progressively unrolled during the factorization and therefore the DAG size is limited as well as the memory consumption
• less eager than the qr_mumps scheduler
• the assembly tasks are serialized and are executed in order of submission although it is unnecessary. Need a commute flag in StarPU for commutative operations
Experimental setup

- **Platform:**
  - 4× AMD hexacore
  - 76 GB of memory (in 4 NUMA modules)
  - GNU 4.4 compilers
  - MKL 10.2

- **Problems:** a set of matrices from the UF collection

<table>
<thead>
<tr>
<th>#</th>
<th>Matrix</th>
<th>m</th>
<th>n</th>
<th>nnz</th>
<th>flops</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>tp-6</td>
<td>142752</td>
<td>1014301</td>
<td>11537419</td>
<td>255 G</td>
</tr>
<tr>
<td>2</td>
<td>karted</td>
<td>46502</td>
<td>133115</td>
<td>1770349</td>
<td>258 G</td>
</tr>
<tr>
<td>3</td>
<td>EternityII_E</td>
<td>11077</td>
<td>262144</td>
<td>1572792</td>
<td>544 G</td>
</tr>
<tr>
<td>4</td>
<td>degme</td>
<td>185501</td>
<td>659415</td>
<td>8127528</td>
<td>591 G</td>
</tr>
<tr>
<td>5</td>
<td>cat_ears_4_4</td>
<td>19020</td>
<td>44448</td>
<td>132888</td>
<td>716 G</td>
</tr>
<tr>
<td>6</td>
<td>Hirlam</td>
<td>1385270</td>
<td>452200</td>
<td>2713200</td>
<td>2401 G</td>
</tr>
<tr>
<td>7</td>
<td>e18</td>
<td>24617</td>
<td>38602</td>
<td>156466</td>
<td>3399 G</td>
</tr>
<tr>
<td>8</td>
<td>flower_7_4</td>
<td>27693</td>
<td>67593</td>
<td>202218</td>
<td>4261 G</td>
</tr>
<tr>
<td>9</td>
<td>Rucci1</td>
<td>1977885</td>
<td>109900</td>
<td>7791168</td>
<td>12768 G</td>
</tr>
<tr>
<td>10</td>
<td>sls</td>
<td>1748122</td>
<td>62729</td>
<td>6804304</td>
<td>22716 G</td>
</tr>
<tr>
<td>11</td>
<td>TF17</td>
<td>38132</td>
<td>48630</td>
<td>586218</td>
<td>38209 G</td>
</tr>
</tbody>
</table>
Experimental results

Relative performance compared to qr_mumps -- 24 cores

Matrix number

Relative performance compared to qr_mumps -- 24 cores

1.0
0.84

Matrix number

MUMPS Users Group Meeting, May 29-30, 2013
Experimental results

Relative maximum DAG size -- 24 cores

Matrix number

Relative maximum DAG size -- 24 cores

MUMPS Users Group Meeting, May 29-30, 2013
Experimental results

Sequential execution

Parallel execution

Cumulative times ($p$ processors) measured during the factorization:

- reference sequential time $t_c(1)$

Parallel efficiency $e(p)$ ($p$ processors):
Experimental results

Cumulative times ($p$ processors) measured during the factorization:

- reference sequential time $t_c(1)$
- $t_c(p)$: task time

Parallel efficiency $e(p)$ ($p$ processors):
Cumulative times (p processors) measured during the factorization:

- reference sequential time $t_c(1)$
- $t_c(p)$: task time ($\neq t_c(1)$)

Parallel efficiency $e(p)$ (p processors):
Experimental results

Cumulative times (p processors) measured during the factorization:

- reference sequential time $t_c(1)$
- $t_c(p)$: task time ($\neq t_c(1)$)
- $t_i(p)$: idle time

Parallel efficiency $e(p)$ (p processors):
Experimental results

Sequential execution

Parallel execution

Cumulative times (p processors) measured during the factorization:

- reference sequential time \( t_c(1) \)
- \( t_c(p) \): task time \((\neq t_c(1))\)
- \( t_i(p) \): idle time
- \( t_s(p) \): scheduler time

Parallel efficiency \( e(p) \) (p processors):
Experimental results

Cumulative times (p processors) measured during the factorization:

- reference sequential time $t_c(1)$
- $t_c(p)$: task time ($\neq t_c(1)$)
- $t_i(p)$: idle time
- $t_s(p)$: scheduler time

Parallel efficiency $e(p)$ (p processors):

$$e(p) = \frac{t_c(1)}{t_c(p) + t_s(p) + t_i(p)}$$
Experimental results

Efficiency of the parallelism $e(p)$ ($p$ processors) decomposed into three efficiencies:

$$e(p) = \frac{e_l}{t_c(1)} \cdot \frac{e_p}{t_c(p) + t_s(p)} \cdot \frac{e_s}{t_c(p) + t_s(p) + t_i(p)}$$

These efficiencies correspond to the three identified effects:

- $e_l(p)$: locality efficiency
- $e_p(p)$: pipeline efficiency
- $e_s(p)$: scheduler efficiency
Experimental results

Cumulative time for qr_starpu (left) and qr_mumps (right)

Matrix number
Experimental results

Parallelism efficiency $e = e_l \cdot e_s \cdot e_p$ -- 24 cores

- $qr_{\text{starpu}}$
- $qr_{\text{mumps}}$

Efficiencies -- 24 cores

Similar locality efficiencies for both codes.

Higher scheduling overhead for small matrices especially with $qr_{\text{starpu}}$.

Poorer pipeline for $qr_{\text{starpu}}$ mainly due to:
- The serialization of assembly tasks
- The strategy of front activation limiting the parallelism
Experimental results

- **similar locality efficiencies for both codes**
- **higher scheduling overhead** for small matrices especially with **qr_starpu**

- **poorer pipeline for qr_starpu** mainly due to:
  - the serialization of assembly tasks
  - the strategy of front activation limiting the parallelism
Experimental results

- Memory footprint (MB)

Matrix number

- qr_starpu
- qr_mumps
- spqr

MUMPS Users Group Meeting, May 29-30, 2013
Experimental results: conclusion

- qr_starpu achieves a very competitive performance compared to qr_mumps and an excellent memory behaviour
- higher but still marginal scheduling overhead imposed by the runtime system
- good scalability of the runtime system thanks to the adaptive task submission
- minor limitations of StarPU common to many other runtime system environments

This version constitutes a good basis for the development of a multifrontal method for heterogeneous architectures
Ongoing & future work
Ongoing work

- possibility to declare commutative operations in StarPU
- Use GPUs to process the biggest fronts (top of the tree)
- consider other models to express the task graph: Compare the Sequential Task Flow model (STF) of StarPU with the Parametrized Task graph (PTG) model of PaRSEC (collaboration with George Bosilca)
- control the memory consumption with a memory-aware algorithm (shared-memory version of the approach presented by François-Henry Rouet)
- use of scheduling contexts in StarPU (Andra Hugo et al.) to achieve a better data locality.
Future work

- scheduling strategies (use of performance models)
- process the factorization of entire sub-trees on GPUs (potential collaboration with T. Davis)
- 2D front partitioning
- MIC architectures
Thanks!
Questions?
Ongoing work

Use GPUs to process the biggest fronts (top of the tree). MAGMA-like approach: panel operations on CPUs and update on GPUs
Ongoing work

Use GPUs to process the biggest fronts (top of the tree). MAGMA-like approch: panel operations on CPUs and update on GPUs
Ongoing work

Use GPUs to process the biggest fronts (top of the tree). MAGMA-like approach: panel operations on CPUs and update on GPUs.
Ongoing work

Front factorization -- 2 CPUs 1 GPU

Matrix order vs. Gflop/s for different methods:
- MAGMA
- qr_starpu
- basic

The graph shows the performance of different methods as the matrix order increases.