Memory-Aware Scheduling for Sparse Direct Methods

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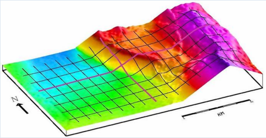
Abdou GUERMOUCHE, LaBRI, Université de Bordeaux
Jean-Yves L'EXCELLENT, LIP - INRIA

May 15, 2009

Context

Solving sparse linear systems



$$Ax = b$$

$\Rightarrow$ Direct methods: $A = LU$

Typical matrix: BRGM matrix

- 3.7×10^6 variables
- 156×10^6 non zeros in A
- 4.5×10^9 non zeros in LU
- 26.5×10^{12} flops

Hardware paradigm

- Many-core architecture.
- Large global amount of memory.
- Limited memory per core.

Software challenge

$\rightarrow$ Need for algorithms whose memory usage scales with the number of processors.

- Case study: MUMPS

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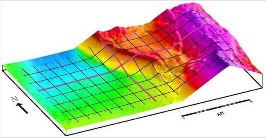

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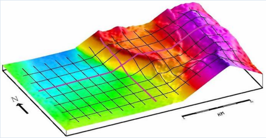

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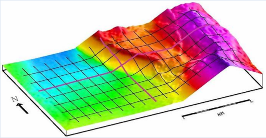

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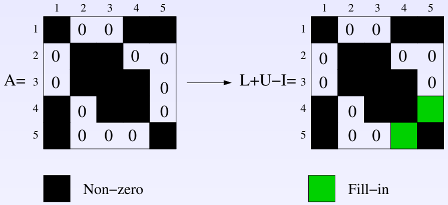

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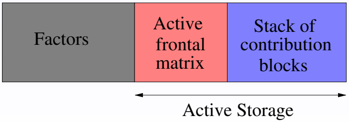

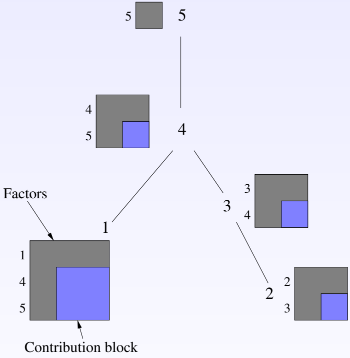

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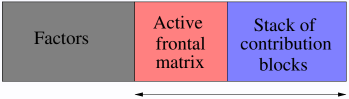

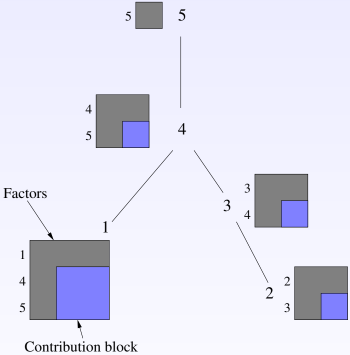

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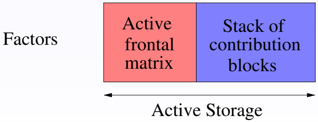

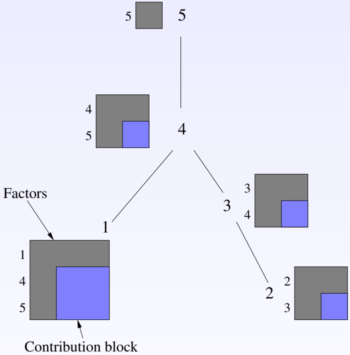

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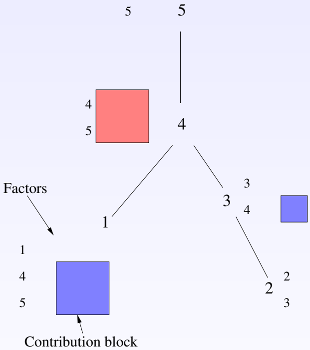

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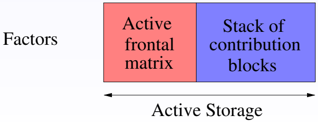

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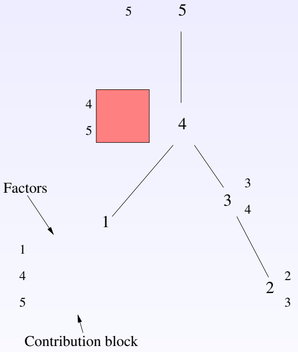

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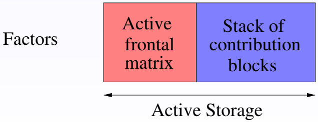

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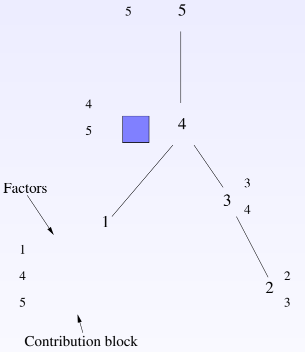

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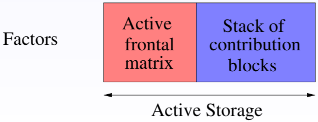

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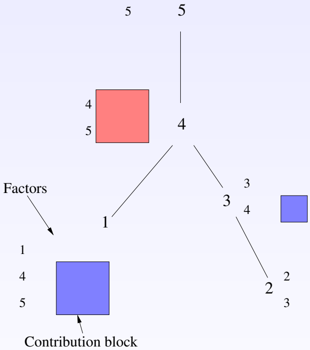

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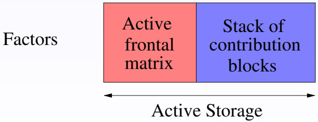

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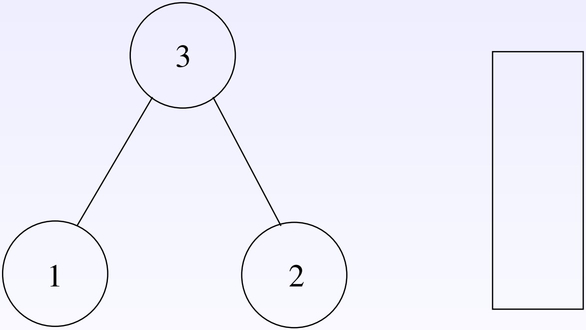
Memory behaviour (serial postorder traversal)



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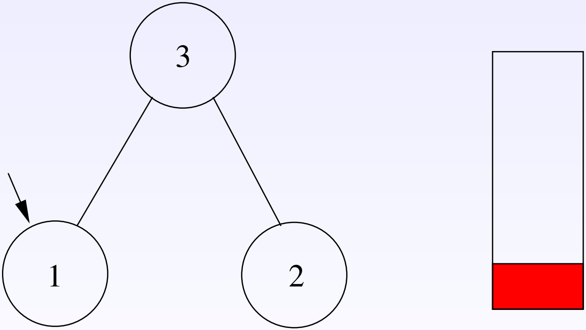

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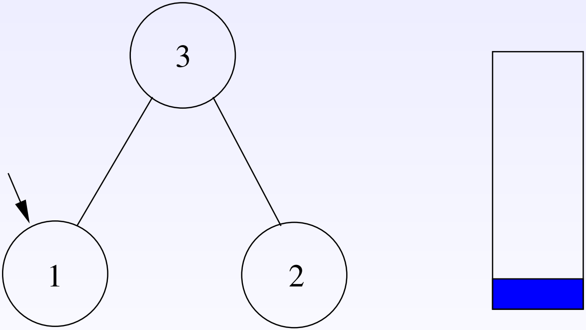

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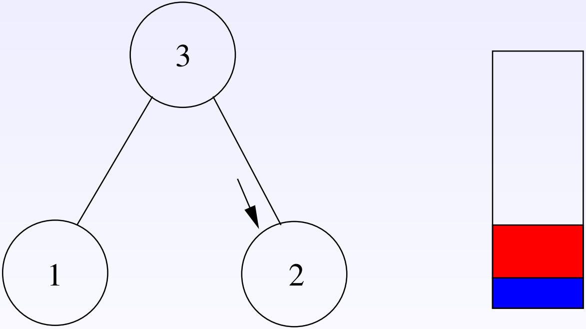

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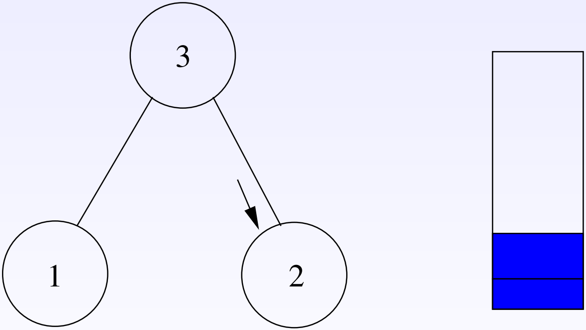

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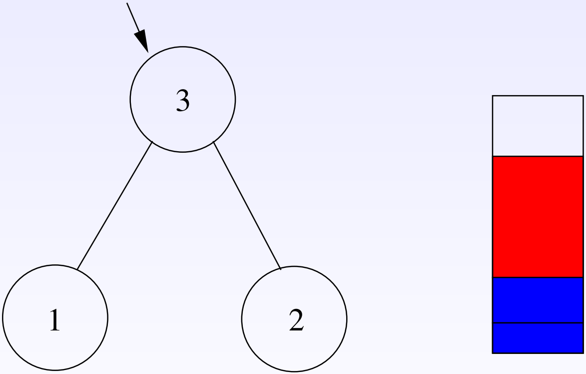

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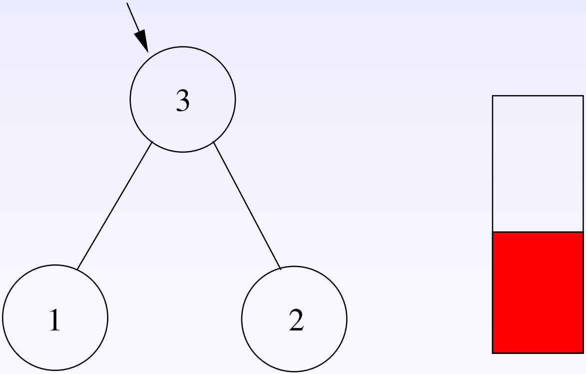

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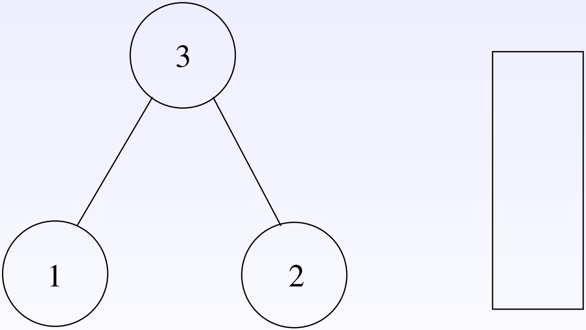

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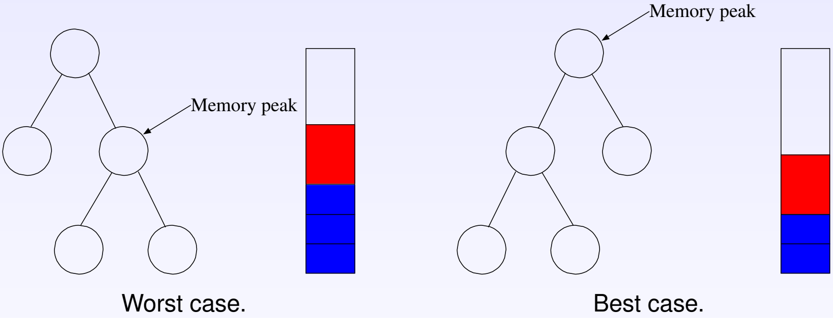

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→ Algorithms to find the optimal tree traversal have been proposed

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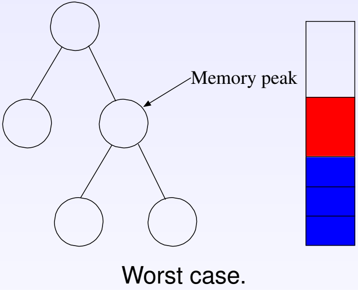

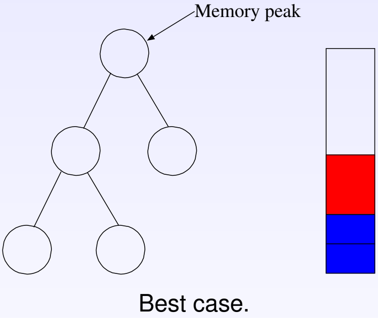

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Memory efficiency

Definition: *Memory Efficiency* on p processors (or cores)

$e(p) = \frac{S_{seq}}{p \times S_{max}(p)}$, S_{seq}: serial storage, S_{max}: parallel storage

Results: Memory Efficiency of MUMPS (with factors on disk)

Number p of processors	16	32	64	128
AUDI_KW_1	0.16	0.12	0.13	0.10
CONESHL_MOD	0.28	0.28	0.22	0.19
CONV3D64	0.42	0.40	0.41	0.37
QIMONDA07	0.30	0.18	0.11	-
ULTRASOUND80	0.32	0.31	0.30	0.26

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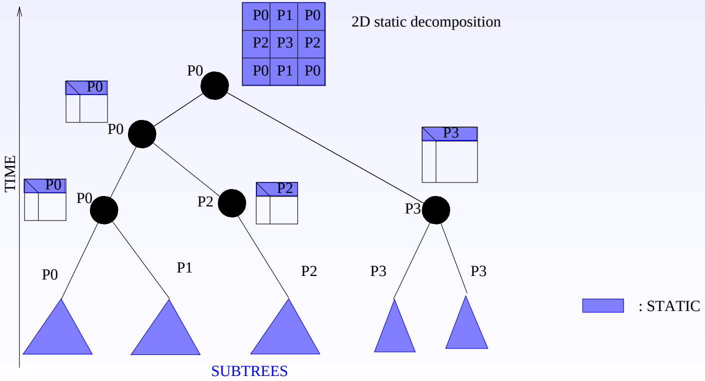
Parallel multifrontal scheme

- **Type 1** : Nodes processed on a single processor
- **Type 2** : Nodes processed with a parallel 1D blocked factorization
- **Type 3** : Parallel 2D cyclic factorization (root node)



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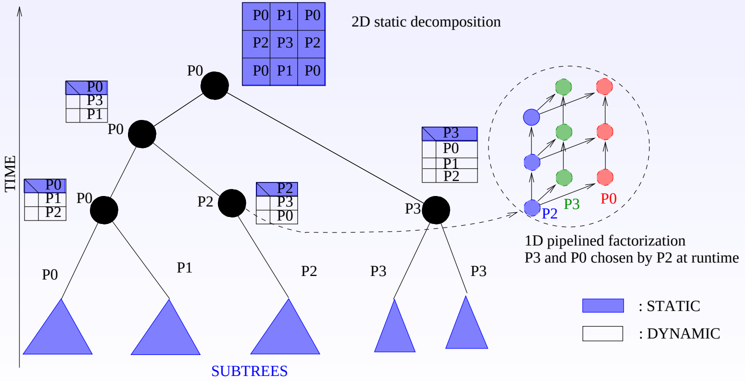

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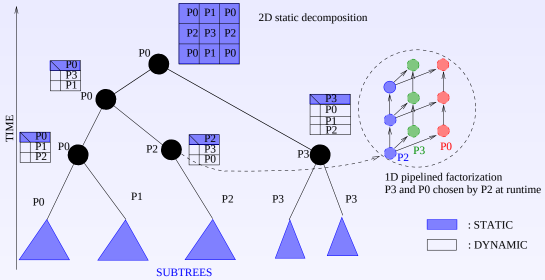

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- Large master tasks;
- Large subtrees;
- Proportional mapping.

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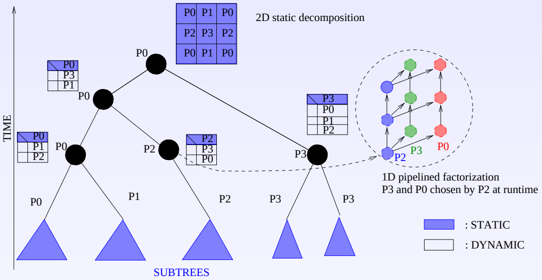

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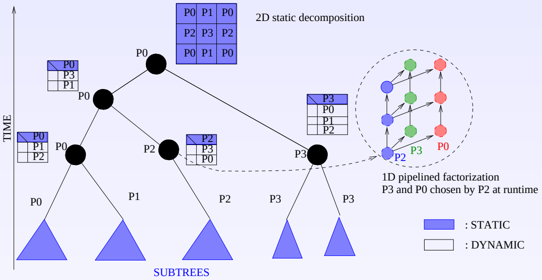

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Proportional mapping VS postorder traversal (1/2)

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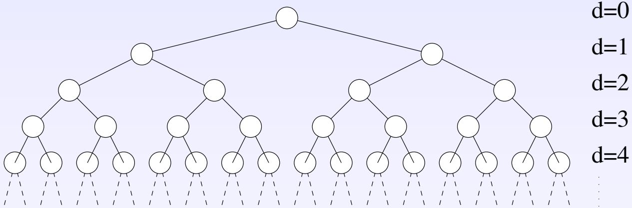

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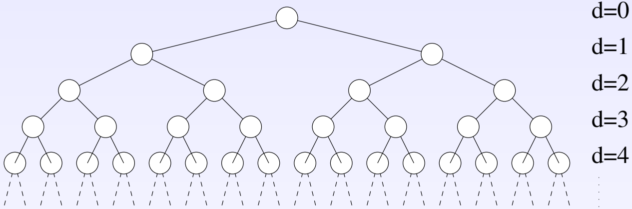

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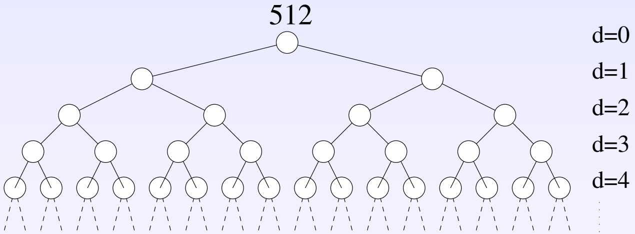

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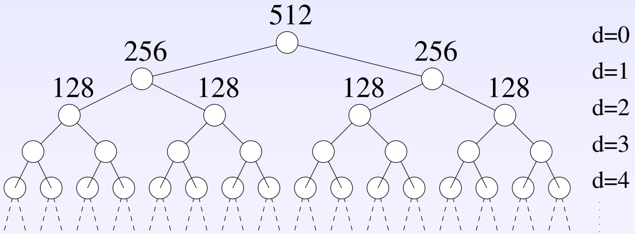

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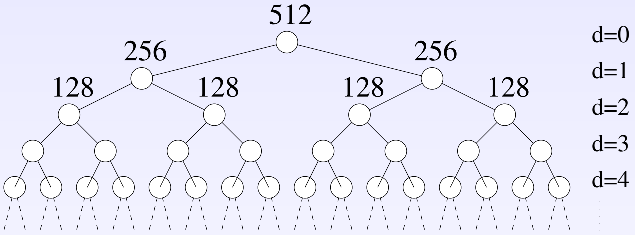

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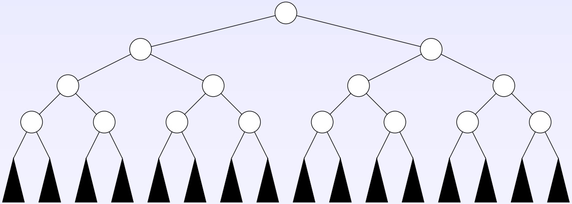

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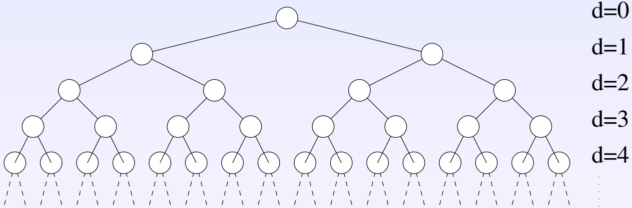

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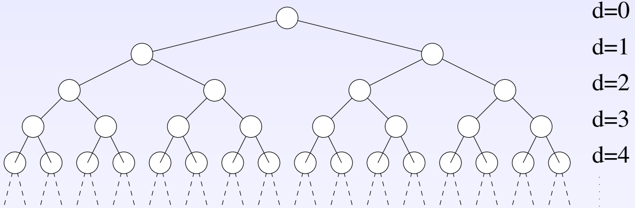

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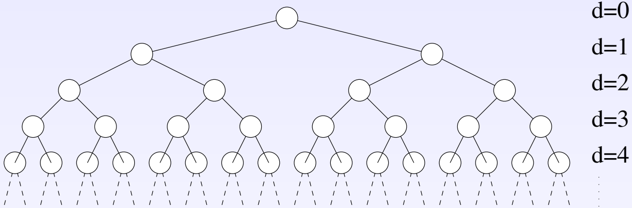

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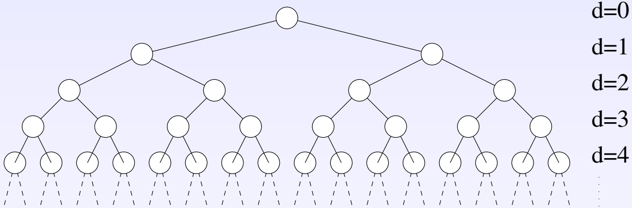

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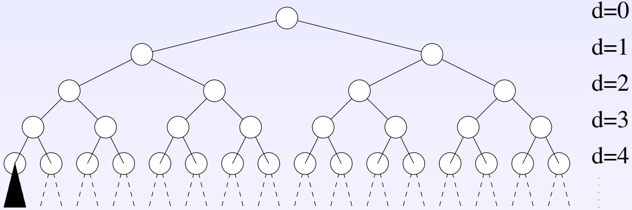

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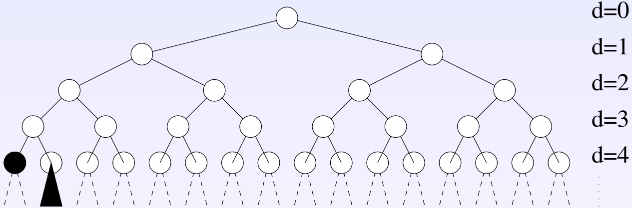

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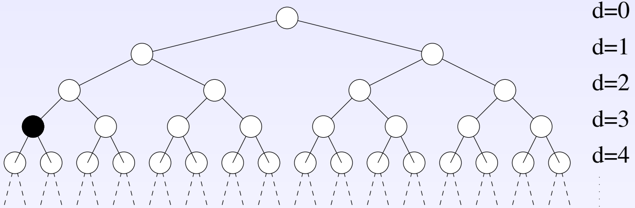

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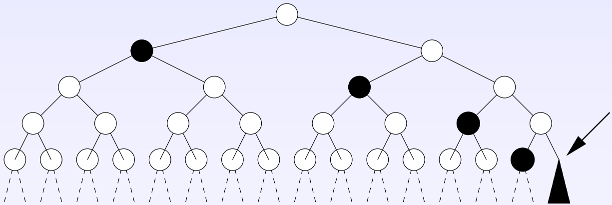

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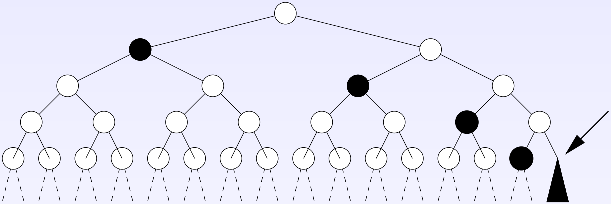

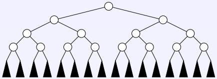

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Proportional mapping VS postorder traversal (2/2)

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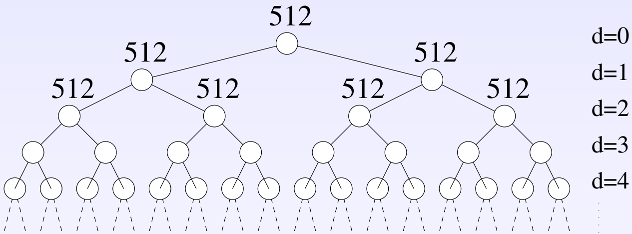


Traversal

- ⋆ Postorder traversal, node by node;
- ⋆ All processors on each node.

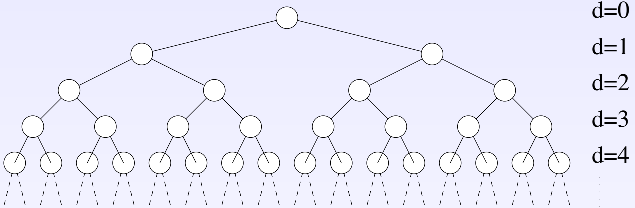
Advantages and drawbacks

- ☹ Only task-level parallelism;
- ☺ High memory efficiency.

Outline

Memory-aware mapping algorithm

Elimination tree :

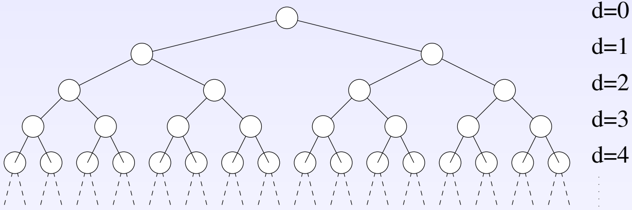


Mapping

- Initially: all processors on root node;
- Recursively split the set of processors on child subtrees if memory allows for it.

Memory-aware mapping algorithm

Memory-aware mapping:



Mapping

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Memory-aware mapping algorithm

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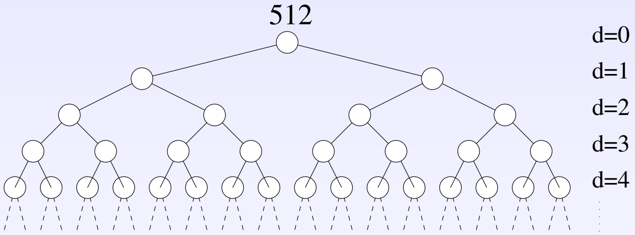

Mapping

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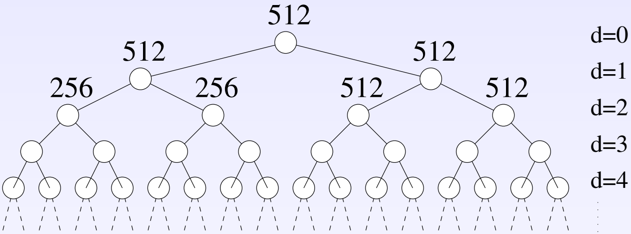
Memory-aware mapping algorithm

Memory-aware mapping:



Mapping

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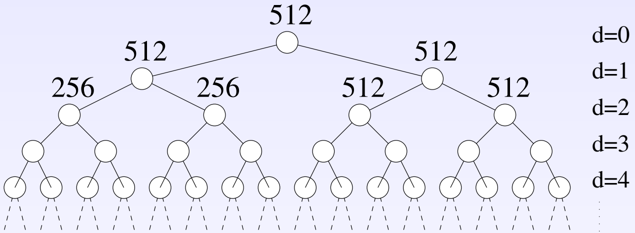
Memory-aware mapping algorithm

Memory-aware mapping:



Advantages

- ☺ Robust: guaranteed (if memory $M_0 < \frac{S_{seq}}{p}$).
- ☺ Efficient: available memory provides tree-level parallelism.

Outline

MUMPS: a MUltifrontal Massively Parallel sparse direct Solver

Solution of large sparse linear systems with:

- ⋆ Symmetric positive definite matrices;
- ⋆ General symmetric matrices;
- ⋆ General unsymmetric matrices.

Implementation

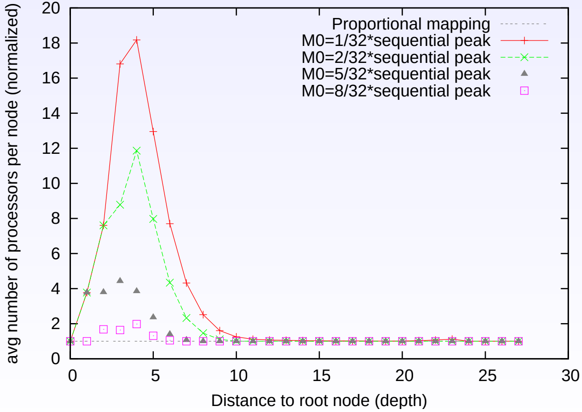
- ⋆ Distributed Multifrontal Solver (F90, MPI based);
- ⋆ Dynamic Distributed Scheduling;
- ⋆ Use of BLAS, BLACS, ScaLAPACK.

Interfaces

- ⋆ Fortran, C, Matlab, Scilab, Visual Studio.

Preliminary results

- Excellent memory scalability:
  - memory efficiency closed to 1.
- Competitive (time) efficiency
  - closed to proportional mapping (if enough memory);
  - memory provides tree-level parallelism:



Outline

Conclusion

Prototype of a *memory-aware* algorithm

- ⋆ Maximizes the amount of tree-level parallelism with respect to the amount of memory available per processor/core.
- ⋆ New static mapping implemented, with constraints on dynamic schedulers; experimented within the OOC version of MUMPS.
- ⋆ Very good memory scalability obtained.

On-going work

- ⋆ Further tuning and validation.
- ⋆ Generalization to the in-core case.
- ⋆ Reinject dynamic information to schedulers.