CURRICULUM VITAE

Yves Robert

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Contents

1 Executive Summary

1.1 Past and current employment

Contact information

Position: Full Professor of Computer Science, Ecole Normale Supérieure de Lyon, France
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Education

Agrégation de Mathématiques, 1980
Ph.D. Thesis, Applied Mathematics, Université de Grenoble, France, 1982
Doctorat es Sciences (Habilitation), Computer Science, Institut National Polytechnique de Grenoble, France, 1986

Professional appointments

Permanent Researcher at CNRS, 1983-1988
Professor, Ecole Normale Supérieure de Lyon, 1988-present
Professor of exceptional class since 2003 – highest position of the French system
Visiting Scientist, IBM ECSEC Rome, 1986-1987 (contributed to the ESSL scientific library)
Visiting Professor, Univ. Tennessee Knoxville, 1996-1997 (contributed to ScaLAPACK)
Adjunct Professor at Ecole Polytechnique Paris, 1999-2001
Visiting Scientist, Univ. Tennessee Knoxville, 2011-present (algorithms and fault-tolerance at scale)
Institut Universitaire de France (IUF)[1]: junior member, 1993–1998 and senior member, 2007-2017

1.2 Professional achievements

Academic responsibilities

Head of CNRS–INRIA project *ReMaP*, 1995-2000
Head of Computer Science postgraduate studies at ENS Lyon, 1989-1995, and 2004-2007
Vice-head, then head of LIP, the computer science lab. of ENS Lyon, 1993-1997 and 1997-2001
Head of Computer Science Department at ENS Lyon, 2005-2008
INRIA executive director for JLESC, the Joint Laboratory for Extreme Scale Computing (with ANL, BSC, JSC, Riken, UIUC and UTK), 2014–present

Research and publications

- Research topics: parallel algorithms, scheduling techniques, resilience
- 163 papers in international journals, 240 papers in international conferences. See complete publication list in Section 4
- Organization of several conferences, editing of 11 proceedings and 15 journal special issues

[1] IUF is a prestigious institution that grants reduced teaching load (one third) and special funding to University Professors from all over France. There are around 30 senior members from all scientific and humanities disciplines elected each year, for a duration of 5 years. When elected in 2007, I was the only Computer Scientist of all IUF senior members.

- H-index: 52; citations: 10,356 (according to Google Scholar)

Student supervision

- Advisor of 33 completed and 4 on-going PhD theses
- Current position of the 33 former PhD students: 7 Full Professors, 4 Senior Researchers at CNRS or INRIA, 11 Associate Professors, 5 Permanent Researchers at CNRS or INRIA, 4 Engineers, 2 Post-doctorate
- Participation to 115 PhD and 25 Habilitation defense committees

Teaching

- Institutions: ENS Lyon, INP Grenoble, Ecole Polytechnique Paris, EPFL Lausanne, University of Tennessee at Knoxville, ECNU Shanghai
- Pedagogical documents: 7 books, several class notes. Last monographs:
  - H. Casanova, A. Legrand, and Y. Robert. *Parallel Algorithms.* Chapman & Hall/CRC Press, 2008
  - Y. Robert and F. Vivien, editors. *Introduction to Scheduling.* Chapman & Hall/CRC Press, 2009
  - A. Benoit, Y. Robert and F. Vivien. *A guide to algorithm design: paradigms, methods, and complexity analysis*, Chapman & Hall/CRC Press, 2013
  - T. Hérault and Y. Robert, editors, *Fault-tolerance techniques for high-performance computing*, Springer Verlag, 2015

Service to the Profession

- Former editorial board member of *Integration, the VLSI journal*, *Parallel Processing Letters*, *IEEE Trans. Parallel and Distributed Systems* and *JPDC (J. Parallel Dist. Computing)*. Current editorial board member of *ACM TOPC (Trans. On Parallel Computing)*, *Int. J. High Performance Computing Applications*, *Journal of Computational Science* and *Int. J. Grid and Utility Computing.*
- Responsibilities in recent program committees:
  - Program chair of HCW 2004 (IEEE Heterogeneous Computing Workshop), HiPC 2006 (IEEE Int. Conf. on High Performance Computing), IPDPS 2008 (IEEE Int. Parallel and Distributed Processing Symposium), ISPDC 2009 (International Symposium on Parallel and Distributed Computing), ICPP 2013 (Int. Conference on Parallel Processing) and HiPC 2013 (High Performance Computing)
  - Program vice-chair of ICPP 2011, IPDPS 2003, 2005 and 2007, SC 2004 and 2014 (ACM Super Computing), ICPADS 2006 and 2008, HiPC 2012
  - Panels Chair at SC 2017
  - Steering committee member of IPDPS, HCW and HeteroPar
- President of the Computer Science hiring committee of ENS Lyon, 2001-2005 Member of several such hiring committees across France
- Member, IEEE Fellow Selection Committee, 2012-present. Vice-president of the Committee, 2014
- Parallel and distributed computing curriculum: since 2009, I have been involved in the NSF/TCPP initiative on the parallel and distributed computing (PDC) curriculum (see `http://www.cs.gsu.edu/~tcpp/curriculum/index.php`)

Major funding

- EC Project Esprit BRA 3280 "NANA" and Esprit III BRA "NANA2", 1989-1995
- Scientific Director of LHPC, joint laboratory for high performance computing with Matra (now Lagardère group), 1994-2002, managing several EC contracts (EuroTOPS PARALIN, ProxyTV) and contracts with *Ministère de l'Industrie* (CHARM, SPIHD)
- Head of TTN ProHPC, European center for the transfer of parallel computing technology to SMEs, 1997-1999
- Head of two white research contracts for the French Research Agency ANR: StochaGrid (2008-2010) and Rescue (2011-2014)
- Head of collaboration program with ECNU Shanghai, 2015-present

Recent talks

- Keynote talk at IPDPS'2006 (Rhodes), ICCS'2007 (Beijing), HCW'2011 (Anchorage), ExaComp'2011 (Seoul), ExaComp'2013, IC3'2013 (New Delhi), P2S2'2013 (Lyon), CCGrid'2014 (Chicago), HiPC'2014 (Goa), FTS'2017 (Honolulu), SBACPAD'2018 (Lyon), HPCS'2019 (Dublin)
- 40+ invited talks in various US universities since 2010

1.3 Awards and distinctions

- 3rd Price IBM France "Intensive Numerical Computing", 1988
- Bronze Medal of CNRS, 1988
- Grand Prix Informatique IBM France, 1991
- IEEE Fellow, *for contributions to the design and analysis of parallel algorithms and scheduling techniques*, 2005
- IEEE TCSC Award of Excellence in Scalable Computing, *for outstanding contributions to parallel algorithms, scheduling techniques and resilience methods for large-scale distributed systems*, 2014
- IEEE TCPP Outstanding Service Award, 2016

2 PhD students

2.1 Former PhD students

1. Mounir Marrakchi, July 6,1988
   Title of PhD thesis: Techniques d'ordonnancement et algorithmique parallèle en algèbre linéaire
   Current position: Full Professor, Riyad University, Saudi Arabia

2. Abedelhamid Benaini, March 22,1990
   Title of PhD thesis: Contribution à l'algorithmique systolique
   Current position: Full Professor, Université du Havre, France

3. Serge Miguet, December 17, 1990
   Title of PhD thesis: Programmation dynamique et traitement d'images sur machines parallèles à mémoire distribuée
   Current position: Full Professor, Université Lyon 2, France

4. Jian-Jin Li, pril 21, 1992
   Title of PhD thesis: Algorithmes parallèles pour la synthèse d'image sur machines à mémoire distribuée
   Current position: Associate Professor, Université de Clermont-Ferrand, France

5. Stéphane Ubéda, February 5, 1993
   Title of PhD thesis: Algorithmes d'amincissement d'images sur machines parallèles
   Current position: Full Professor, INSA Lyon, France

6. Henri-Pierre Charles, February 12, 1993
   Title of PhD thesis: De la micro-optimisation à l'algorithmique parallèle
   Current position: Full Professor, Université de Versailles, France St Quentin

7. Alain Darte, April 21, 1993
   Title of PhD thesis: Techniques de parallélisation de nids de boucles
   Current position: Senior Researcher, CNRS, LIP ENS Lyon, France

8. Tanguy Risset, February 1, 1994
   Title of PhD thesis: Parallélisation automatique : du modèle systolique à la compilation des nids de boucles
   Current position: Full Professor, INSA Lyon, France

9. Laurent Perroton, December 5,1994
   Title of PhD thesis: Segmentation parallèle d'images volumiques
   Current position: Associate Professor, ESIEE Marne la Vallée, France

10. Virginie Poty, December 9, 1994
    Title of PhD thesis: Approches parallèles pour la squelettisation 3D
    Current position: Associate Professor, Université du Littoral, France

11. Pierre Boulet, January 18, 1996
    Title of PhD thesis: Outils pour la parallélisation automatique
    Current position: Full Professor, Université de Lille

12. Michèle Dion, January 18, 1996
    Title of PhD thesis: Alignement et distribution en parallélisation automatique
    Current position: Chief Engineer, EDF, Clamart, France

13. Laurent Lefèvre, January 8, 1997
    Title of PhD thesis: Conception et mise en oeuvre d'un environnement de programmation parallèle fondé sur un système de mémoire distribuée virtuellement partagée
    Current position: Permanent Researcher, INRIA, LIP ENS Lyon, France

14. Pierre-Yves Calland, December 17, 1997
    Title of PhD thesis: Contributions aux techniques d'optimisation en compilation des programmes parallèles
    Current position: Associate Professor, Université de Valenciennes, France

15. Frédéric Vivien, December 17, 1997
    Title of PhD thesis: Détection de parallélisme dans les boucles imbriquées
    Current position: Senior Researcher, INRIA, LIP ENS Lyon, France

16. Cyril Randriamaro, January 24, 2000
    Title of PhD thesis: Optimisation des redistributions et allocation dynamique en parallélisme de données
    Current position: Associate Professor, Université d'Amiens, France

17. Fabrice Rastello, September 6, 2000
    Title of PhD thesis: Partitionnement: optimisations de compilation et algorithmique hétérogène
    Current position: Senior Researcher, INRIA, Grenoble, France

18. Vincent Boudet, December 21, 2001
    Title of PhD thesis: Stratégies statiques (algorithmique et ordonnancement) pour plateformes hétérogènes
    Current position: Associate Professor, Université de Montpellier, France

19. Arnaud Legrand, December 11, 2003
    Title of PhD thesis:Algorithmique parallèle hétérogène et techniques d'ordonnancement: approches statiques et dynamiques
    Current position: Senior Researcher, CNRS, LIG Grenoble, France

20. Hélène Renard, December 13, 2005
    Title of PhD thesis:Equilibrage de charge pour algorithmes itératifs sur plates-formes hétérogènes
    Current position: Associate Professor, Université de Nice Sophia-Antipolis, France

21. Loris Marchal, October 17, 2006
    Title of PhD thesis:Macro-communications sur plates-formes distribuées à grande échelle
    Current position: Permanent Researcher, CNRS, LIP ENS Lyon, France

22. Jean-François Pineau, September 25, 2008
    Title of PhD thesis: Communication-aware scheduling on heterogeneous master-worker platforms
    Current position: Engineer, Demand Side Instruments, Switzerland

23. Veronika Rehn, July 7, 2009 Title of PhD thesis: Multi-criteria mapping and scheduling of workflow applications onto heterogeneous platforms
Current position: Associate Professor, Université de Franche-Comté, France

24. Matthieu Gallet, October 20, 2009 Title of PhD thesis: Steady-state scheduling on heterogeneous platforms
Current position: Engineer, DGA Paris, France

25. Mathias Jacquelin, July 20, 2011 Title of PhD thesis: Memory-aware algorithms: from multicore processors to large scale platforms
Current position: Researcher, LBNL Berkeley, USA

26. Fanny Dufossé, September 6, 2011
Title of PhD thesis: Scheduling for reliability: complexity and algorithms
Current position: Permanent Researcher, INRIA, Grenoble, France

27. Paul Renaud-Goud, July 5, 2012
Title of PhD thesis: Energy-aware scheduling: complexity and algorithms
Current position: Associate Professor, IRIT Toulouse, France

28. Guillaume Aupy, September 16, 2014
Title of PhD thesis: Resilient and energy-efficient scheduling algorithms at scale
Current position: Permanent Researcher, INRIA Bordeaux, France

29. Dounia Zaidouni, December 10, 2014
Title of PhD thesis: Combining checkpointing and other resilience mechanisms for exascale systems
Current position: Associate Professor, INPT Rabat, Morocco

30. Julien Herrmann, November 15, 2015
Title of PhD thesis: Algorithms and Scheduling Techniques for Matrix Computations November 2015
Current position: Post-doc, INRIA Bordeaux, France

31. Aurélien Cavelan, July 7, 2017
Title of PhD thesis: Algorithms for the detection and correction of silent errors
Current position: Post-doc, Basel University, Switzerland

32. Oguz Kaya, September 15, 2017
Title of PhD thesis: High Performance Parallel Algorithms for Tensor Decompositions.
Current position: Associate Professor, LRI Paris, France

33. Loic Pottier , September 18, 2018
Title of PhD thesis: Co-scheduling for large-scale applications: memory and resilience Current position: Post-doc, Information Sciences Institute (USC), Los Angeles, USA

2.2 Current PhD students

1. Li Han (since October 2016)
   Title of PhD thesis: Resilience for workflows at scale

2. Aurélie Kong Win Chang (since October 2016)
   Title of PhD thesis: Multi-criteria scheduling on cloud platforms

3. Valentin Le Fèvre (since October 2017)
   Title of PhD thesis: Fault-tolerant algorithms at scale

4. Yiqin Gao (since October 2018)
   Title of PhD thesis: Scheduling workflows on cloud platforms

5. Yishu Du (since October 2019)
   Title of PhD thesis: Fault-tolerant iterative algorithms for sparse linear algebra

2.3 Position of former PhD students

Here is a summary table of the current position held my former 33 PhD students:

Position	Number
Full Professor	7
Senior Researcher (CNRS, INRIA)	5
Associate Professor	11
Junior Researcher (CNRS, INRIA)	4
Engineer/Researcher	3
Post-doc	3

3 Technical Contributions

3.1 Overview

The main theme of my research is *resource optimization*: models, algorithms, and scheduling.

Modern computing platforms provide huge amounts of computational power –the top supercomputers contain more than 100,000 cores, and volunteer computing grids gather millions of processors. Despite the advent of such large and ubiquitous computing facilities, my core belief is that algorithm design and scheduling techniques remain fully useful, not to say unavoidable. The more resources at our disposal, the more difficult the art of selecting which ones to enroll in the execution, and of mapping the right task onto the right machine. My research project focuses on enabling scientific computing applications to fully harness modern computing platforms, through: (i) the design of multi-criteria optimizations which both guarantee the efficiency of platform usage and some QoS (Quality of Service) for users; (ii) the design of static approaches able to cope with platform dynamicity; and (iii) the design of resilient algorithms for very large-scale (hence heavily failure-prone) platforms.

I have been active in the field of parallel algorithms and scheduling techniques since 1982. I have studied cellular automata, systolic algorithms and architectures, parallel algorithms for distributed-memory computers, communication and redistribution routines, loop transformations, mapping and tiling strategies, task graph scheduling, steady-state scheduling, workflow scheduling, and more recently energy-aware scheduling, numerical linear algebra kernels, and resilience methods at scale. Most of my research has dealt with scalable parallel algorithms, from systolic arrays and hypercubes up to multicore clusters.

During these 35+ years, I have written 7 books, edited 11 monographs and proceedings, and 15 special issues. I have published 163 journal papers and 240 conference papers. The complete list of my publications is given in Section 4. In order to provide an overview of my activity over all these years, I am summarizing my key research achievements below. Also, I am listing 10 major publications, whose selection is somewhat arbitrary, but I tried to pick a representative sample, with 7 research papers, 1 edited monograph and 2 books. Abstracts of these 10 publications, together with some comments on their impact, are also provided below.

3.2 Key research achievements

My key contributions lie in three (inter-related) areas: parallel algorithms (for quite a variety of platforms), parallelizing compilers (loop-nest transformations and polyhedral model), and scheduling techniques (task graphs, pipelined workflows, resilience methods).

Parallel algorithms (design, analysis and complexity)

- Dense linear algebra kernels on shared-memory machines, distributed-memory platforms (rings, grids and hypercubes), and multi-core clusters
- Systolic arrays for string processing, graph theory and matrix computations
- Characterization of optimal block-cyclic distributions for dense linear algebra kernels
- Design and implementation of sparse iterative solvers for the IBM 3090 vector multiprocessor (ESSL scientific library)
- Design and implementation of optimal block-cyclic redistribution algorithms for ScaLAPACK

Parallelizing compilers

- Space-time optimal systolic arrays
- Optimal scheduling of loop nests with uniform and affine dependences
- Mapping, tiling and partitioning techniques for loop nests

Scheduling

- Scheduling algorithms for task graphs and pipelined workflows
- Scheduling collective communications (broadcast, scatter, reduce) on various platforms
- Steady-state scheduling for master/worker (centralized and distributed)
- Multi-criteria scheduling for streaming applications (various objectives chosen as a subset of throughput, latency, reliability, and energy)
- Models and optimal strategies for several checkpointing protocols (possibly coupled with migration, replication, or fault prediction)

According to Google Scholar (which does not allow to discriminate self-citations, and as of September 12, 2019), my papers have been cited 10,356 times, and my H-index is 52. I understand that these numbers are not fully representative of the impact of my research but they are representative of my visibility in the community. According to `http://www.guide2research.com/scientists/FR`, I am ranked as the 43st top H-index computer scientist in France.

My motto is the following: always (try to) combine models and complexity analysis with efficient and practical algorithmic solutions. But it is never easy to predict the impact of your results! To give an example, I have no idea on how many compiler tools and prototypes in the world are currently using our loop nest transformation with Hermite decomposition (see major publication (3)), but this pioneering idea turned out to be the right concept and its impact has been unexpectedly high. Similarly, the intricate proof that the greedy algorithm is optimal for QR decomposition (see major publication (1)) was mostly a theoretical result when published, but multi-core systems have suddenly made this algorithm very important in practice, 30 years later, and I expect its impportance to dramatically increase (while I understand that this 'comeback' is kind of lucky). I could say the same for systolic array algorithms and tiling/partitioning techniques, which had been almost forgotten before coming back due to the (long awaited) advent of massively parallel architectures.

3.3 Major publications

I summarize below the content of 10 major journal publications. When quoting another of my publications, I use [Jxx] to refer to journal number XX in Section 4.4 and [Cyy] to refer to conference number YY in Section 4.5.

(1) Complexity of parallel QR factorization Michel Cosnard and Yves Robert, Journal of the A.C.M. 33, 4 (1986), 712–723.

In this paper, an optimal algorithm to perform the parallel QR decomposition of a dense matrix of size $m \times n$ is presented. Some parallel algorithms had been proposed in the literature, by Sameh and Kuck, and by Modi and Clarke, but no complexity result was known. The asymptotic optimality of the greedy algorithm introduced in this paper is established for square matrices (m = n), and has been extended [J12] to a wide class of matrix size parameters, including the important case (for least squares) where m and n are proportional. This pioneering work was a theoretical breakthrough, and has been followed by a series of papers on the complexity of parallel numerical linear algebra kernels. However, at that time, it has little practical impact, because the model did not take communication costs into account. Things have dramatically changed with the advent of blocked algorithms for factoring tall and skinny matrices on multicore platforms. We have recently incorporated the greedy algorithm into a hierarchical algorithm that represents the state-of-the-art of QR factorization for multi-core platforms, both for shared memory [C177] and distributed memory machines [J125].

(2) Data allocation strategies for the Gauss and Jordan algorithms on a ring of processors Yves Robert, Bernard Tourancheau, and Gilles Villard, Information Processing Letters 31 (1989), 21–29.

In this paper, we discuss various data allocation strategies for the parallel implementation of the Gauss and Jordan algorithms on a ring of processors. For the first time, trade-offs between block distributions, which minimize the volume of communications, and cyclic distributions, which better load-balance computations, are investigated. On the experimental side, we characterize the best block-cyclic, or CYCLIC(r), distribution, for various matrix sizes. On the theoretical size, we provide analytical formulas to compute the optimal distribution as a function of the architecture computation-to-communication ratio. Twenty years later, these results may seem well natural, or well-expected. However, the impact of this paper turned out very important, as it laid the foundations of bloc-cyclic distribution techniques, which are now routinely and extensively used in ScaLAPACK, the reference library. A related result is the design of optimal algorithms for CYCLIC(r) to CYCLIC(s) distributions [J68].

(3) Constructive methods for scheduling uniform loop nests Alain Darte and Yves Robert, IEEE Trans. Parallel Distributed Systems 5, 8 (1994), 814–822.

This paper surveys scheduling techniques for loop nests with uniform dependencies. We have proposed a unified framework to analyze various transformations known as loop interchange or loop skewing, that were only partially understood and analyzed in some particular framework. Our approach extends the hyperplane method and related variants by using a different affine scheduling for each statement within the nest. We have provided a new, constructive, and efficient method (based upon linear programming and Hermite normal form) to determine optimal solutions, i.e., schedules whose total execution time is minimum. This paper is representative of my work on automatic parallelization techniques with the polyhedral model.

(4) Scheduling strategies for master-slave tasking on heterogeneous processor platforms Cyril Banino, Olivier Beaumont, Larry Carter, Jeanne Ferrante, Arnaud Legrand, and Yves Robert, IEEE Trans. Parallel Distributed Systems 15, 4 (2004), 319–330.

According to Google Scholar, this is my journal paper with the largest number of citations. We consider the problem of allocating a large number of independent, equal-sized tasks to a heterogeneous computing platform. We use a non-oriented graph to model the platform, where resources can have different speeds of computation and communication. Because the number of tasks is large, we focus on the question of determining the optimal steady state scheduling strategy for each processor (the fraction of time spent computing and the fraction of time spent communicating with each neighbor). In contrast to minimizing the total execution time, which is NP-hard in most formulations, we show that finding the optimal steady state can be solved using a linear programming approach and, thus, in polynomial time. Our result holds for a quite general framework, allowing for cycles and multiple paths in the interconnection graph, and allowing for several masters. We also consider the simpler case where the platform is a tree. While this case can also be solved via linear programming, we show how to derive a closed form formula to compute the optimal steady state, which gives rise to a bandwidth-centric scheduling strategy. The advantage of this approach is that it can directly support autonomous task scheduling based only on information local to each node; no global information is needed. Finally, we provide a theoretical comparison of the computing power of tree-based versus arbitrary platforms. This paper is representative of my work on steady-state scheduling.

(5) Mapping pipeline skeletons onto heterogeneous platforms Anne Benoit and Yves Robert, J. Parallel and Distributed Computing 68, 6 (2008), 790–808.

This paper brings a new vision for mapping pipelined applications onto heterogeneous execution platforms. Mapping applications onto parallel platforms is a challenging problem, that becomes even more difficult when platforms are heterogeneous, nowadays a standard assumption. We have studied the problem of mapping pipeline skeletons onto different types of platforms: Fully Homogeneous platforms with identical processors and interconnection links; Communication Homogeneous platforms, with identical links but different speed processors; and finally, Fully Heterogeneous platforms. We have established new theoretical complexity results for different mapping policies: a mapping can be required to be one-to-one (a processor is assigned at most one stage), or interval-based (a processor is assigned an interval of consecutive stages), or fully general. One major contribution is the proof that determining the optimal interval-based mapping is NP-hard for Communication Homogeneous platforms, and this result assesses the complexity of the well-known chains-to-chains problem for different-speed processors, which was left open for many years. This paper establishes for the first time the difficulty of dealing with heterogeneous resources, thus extending, 12 years later, the pioneering work of Subhlok and Vondran in a homogeneous setting. After this paper, we have further studied streaming applications, with a multi-criteria optimization approach that combines performance-related objectives (throughput, latency, reliability) and environmental ones (energy minimization).

(6) A survey of pipelined workflow scheduling: models and algorithms Anne Benoit, Umit Catalyurek, Yves Robert, and Erik Saule, ACM Computing Surveys 45, 4 (2013), article 50.

This paper has appeared in the ACM Computing Surveys, the most prestigious forum to publish a survey on an important topic that has received considerable attention in the recent years. Our survey studies pipelined workflows, which represent a large class of applications which need to execute the same workflow on different datasets of identical size. Video processing is a typical example, where each frame undergoes a series of computational manipulations (for filtering and rendering). The efficient execution of such applications necessitates intelligent distribution of the application components and tasks on a parallel machine, and the execution can be orchestrated by utilizing task, data, pipelined, and/or replicated parallelism. The scheduling problem that encompasses all of these techniques is called pipelined workflow scheduling, and it had been widely studied in the last decade. Multiple models and algorithms have flourished to tackle various programming paradigms, constraints, machine behaviors, or optimization goals. Our article surveys the field by summing up and structuring known results and approaches.

(7) Checkpointing and fault prediction Guillaume Aupy, Yves Robert, Frédéric Vivien and Dounia Zaidouni, J. Parallel and Distributed Computing 74, 2 (2014), 2048–2064.

This paper deals with the impact of fault prediction techniques on checkpointing strategies. We extend the classical first-order analysis of Young and Daly in the presence of a fault prediction system, characterized by its recall and its precision. In this framework, we provide optimal algorithms to decide whether and when to take predictions into account, and we derive the optimal value of the checkpointing period. These results allow to analytically assess the key parameters that impact the performance of fault predictors at very large scale. This paper is representative of my recent work on resilience techniques for large-scale systems. We started from the pioneering work of Young and Daly on the checkpointing period, and have extended it in several directions: exact formula for Exponential distributions, both for sequential and parallel jobs [C178], models and formulas for complex protocols [J129] [C188], and combination with prediction (this paper and [C194]).

(8) Assessing general-purpose algorithms to cope with fail-stop and silent errors Anne Benoit, Aurélien Cavelan, Yves Robert, and Hongyang Sun. ACM Trans. Parallel Computing 3, 2 (2016), article 13.

This article combines the traditional checkpointing and rollback recovery strategies with verification mechanisms to cope with both fail-stop and silent errors. The objective is to minimize makespan and/or energy consumption. For divisible load applications, we use first-order approximations to find the optimal checkpointing period to minimize execution time, with an additional verification mechanism to detect silent errors before each checkpoint, hence extending the classical formula by Young and Daly for fail-stop errors only. We further extend the approach to include intermediate verifications, and to consider a bicriteria problem involving both time and energy (linear combination of execution time and energy consumption). Then, we focus on application workflows whose dependence graph is a linear chain of tasks. Here, we determine the optimal checkpointing and verification locations, with or without intermediate verifications, for the bicriteria problem. Rather than using a single speed during the whole execution, we further introduce a new execution scenario, which allows for changing the execution speed via Dynamic Voltage and Frequency Scaling (DVFS). In this latter scenario, we determine the optimal checkpointing and verification locations, as well as the optimal speed pairs for each task segment between any two consecutive checkpoints. Finally, we conduct an extensive set of simulations to support the theoretical study, and to assess the performance of each algorithm, showing that the best overall performance is achieved under the most flexible scenario using intermediate verifications and different speeds. This article is representative of my recent work on silent errors (see [J147] , [J151] and [J156] among others). Silent errors are a major source of concern because they strike undetected, and corrupt results, leading to incorrect application results.

(9) Towards optimal multi-level checkpointing Anne Benoit, Aurélien Cavelan, Yves Robert, and Hongyang Sun. IEEE Trans. Computers 66, 7 (2017), 1212-1226.

This recent paper provides a framework to analyze multi-level checkpointing protocols, by formally defining a k-level checkpointing pattern. We obtain a first-order approximation to the optimal checkpointing period, and show that the corresponding overhead is in the order of $\sum_{\ell=1}^{k} \sqrt{2\lambda_\ell C_\ell}$, where λ_ℓ is the error rate at level ℓ, and C_ℓ the checkpointing cost at level ℓ. This nicely extends the classical Young/Daly formula on single-level checkpointing. Furthermore, we are able to fully characterize the shape of the optimal pattern (number and positions of checkpoints), and we provide a dynamic programming algorithm to determine the optimal subset of levels to be used. Finally, we perform simulations to check the accuracy of the theoretical study and to confirm the optimality of the subset of levels returned by the dynamic programming algorithm. The results nicely corroborate the theoretical study, and demonstrate the usefulness of multi-level checkpointing with the optimal subset of levels. Since multi-level checkpointing seems to be the best protocol for future exascale platforms, we expect that this paper will have a profound impact.

(10) Checkpointing workflows for fail-stop errors Li Han, Louis-Claude Canon, Henri Casanova, Yves Robert and Frédéric Vivien. IEEE Trans. Computers 67, 8 (2018), 1105-1120.

This paper appears this year and represents a major step towards managing workflows in a fault-tolerant environment. More precisely, it considers the problem of orchestrating the execution of workflow applications on parallel computing platforms that are subject to fail-stop failures. The objective is to minimize expected overall execution time, or makespan. A solution to this problem consists of a schedule of the workflow tasks on the available processors and of a decision of which application data to checkpoint to stable storage, so as to mitigate the impact of processor failures. To address this challenge, we consider a restricted class of graphs, Minimal Series-Parallel Graphs (M-SPGS), which is relevant to many real-world workflow applications. For this class of graphs, we propose a recursive list-scheduling algorithm that exploits the M-SPG structure to assign subgraphs to individual processors, and uses dynamic programming to decide how to checkpoint these sub-graphs. We assess the performance of our algorithm for production workflow configurations, comparing it to an approach in which all application data is checkpointed and an approach in which no application data is checkpointed. Results demonstrate that our algorithm outperforms both the former approach, because of lower checkpointing overhead, and the latter approach, because of better resilience to failures. This result beautiful result concludes a line of research that we have been exploring since four of five years, and we expect that this paper will lay the foundations for future work.

3.4 Recent books and monographs

This section provides a brief description of two monographs and two books that I have published in the last 10 years. The table of contents of each of these four manuscripts is attached to my application file.

(1) Introduction to scheduling Yves Robert and Frédéric Vivien editors, Chapman & Hall/CRC Press, 2009.

This monograph has two main objectives: (i) to introduce the basic concepts, methods, and fundamental results of scheduling theory; and (ii) to expose recent developments in the area. In each chapter, emphasis is given to self-contained, easy-to-follow, but still rigorous presentations. The book is full of examples, beautiful theorems, and pedagogical proofs. It also contains an in-depth coverage of some key application fields. Altogether, this book provides a comprehensive overview of important results in the field, organized as a handy reference for students and researchers. It is meant to be accessible to a large audience while covering both the foundations and modern developments.

(2) Parallel algorithms Henri Casanova, Arnaud Legrand and Yves Robert, Chapman & Hall/CRC Press, 2008.

The aim of this book is to provide a rigorous yet accessible treatment of parallel algorithms, including theoretical models of parallel computation, parallel algorithm design for homogeneous and heterogeneous platforms, complexity and performance analysis, and fundamental notions of scheduling. The focus is on algorithms for distributed-memory parallel architectures in which computing elements communicate by exchanging messages. While such platforms have become mainstream, the design of efficient and sound parallel algorithms is still a challenging proposition. Fortunately, in spite of the "leaps and bounds" evolution of parallel computing technology, there exists a core of fundamental algorithmic principles. These principles are largely independent from the details of the underlying platform architecture and provide the basis for developing applications on current and future parallel platforms. This book identifies and synthesizes fundamental ideas and generally applicable algorithmic principles out of the mass of parallel algorithm expertise and practical implementations developed over the last decades.

The book is structured in three distinct parts: Models (chapters 1-3), Parallel Algorithms (chapters 4-6), and Scheduling (chapters 7-8). Chapters 1 and 3 cover two classical theoretical models of parallel computation: PRAMs and sorting networks. Both models provide theoretical foundations for reasoning about parallel algorithms, but also point to particular techniques that can be used to implement efficient parallel algorithms in practice. Chapter 3 discusses network models, both for topology and performance, and defines several classical communication primitives that will serve as the foundations for many of the parallel algorithms presented in the next two chapters. Chapters 4 and 5 discuss parallel algorithms on ring and grid logical topologies, two useful and popular abstractions. Both chapters expose fundamental issues and trade-offs encountered when designing and implementing parallel algorithms in practice. Chapter 6 deals with the issue of load balancing on heterogeneous computing platforms. This topic is highly relevant to emerging computing platforms, for instance, those that aggregate several clusters together. Chapter 7 introduces the notion of scheduling, or the art of orchestrating communication and computation to achieve higher performance. This chapter presents fundamental results and approaches for common scheduling problems that arise when developing parallel algorithms. Chapter 8 describes advanced scheduling topics. These topics include divisible load scheduling and steady-state scheduling, which are crucial because they are directly applicable to the popular master-worker application model. The last section discusses the automatic parallelization of loop nests.

This book is a follow-up of the French version [B5] but has been extensively updated. It has received very good reviews by SIAM Review (issue 52, 1 (2010)) and by HPC Wire (April 2009).

(3) Guide to algorithm design, methods, and complexity analysis Anne Benoit, Yves Robert and Frédéric Vivien, Chapman/CRC Press, 2013.

This book is not meant to be yet another book on algorithm design (there are many good ones already). Instead, it aims at guiding students and researchers who need to solve problems, either by finding optimal algorithms or by assessing new complexity results. In a nutshell, the main objective of this book is to outline the roadmap to follow, and to practice all the corresponding steps, in order to determine the complexity of a problem. Part I aims at training the reader to design efficient algorithms. To do so, we provide a comprehensive set of problems to investigate. Problems are organized along the main design principles (introduction to complexity, divide-and-conquer, Greedy algorithms, Dynamic programming and amortized analysis). Part II deals with NP-completeness and beyond, focusing on polynomial reductions. We deliberately ignore Turing machines and the theoretic arsenal. The (small) price to pay is to admit Cook's theorem, the existence of the canonical NP-complete problem, formula satisfiability, a.k.a. SAT. In Part II, we also cover approaches that go beyond NP-completeness: identifying polynomial instances, approximation algorithms, linear programming, randomized algorithms, branch-and-bound, and backtracking. Part III constitutes the main originality of the book. It is devoted to case studies whose goal is to provide the reader with tools and techniques to assess problem complexity: which instances are polynomial, and which are NP-hard, and what do to for the latter. Part III consists of an introduction summarizing how to assess the complexity of a new problem, and it is illustrated with five case studies: chains-on-chains partitioning, replica placement in tree networks, packet routing matrix product (or tiling the unit square), and online scheduling. These case studies are mostly inspired form the field of parallel and distributed computing.

This book represents a major achievement for me, as it is the outcome of 20+ years of teaching algorithm design and complexity at ENS Lyon.

(4) Fault-tolerance techniques for high-performance computing Thomas Hérault and Yves Robert editors, Springer Verlag, 2015.

This recent monograph presents a comprehensive overview of fault tolerance techniques for high-performance computing (HPC). The text opens with a detailed introduction to the concepts of checkpoint protocols and scheduling algorithms, prediction, replication, silent error detection and correction, together with some application-specific techniques such as ABFT. Emphasis is placed on analytical performance models. This is then followed by a review of general-purpose techniques, including several checkpoint and rollback recovery protocols. Relevant execution scenarios are also evaluated and compared through quantitative models. Features: provides a survey of resilience methods and performance models; examines the various sources for errors and faults in large-scale systems; reviews the spectrum of techniques that can be applied to design a fault-tolerant MPI; investigates different approaches to replication; discusses the challenge of energy consumption of fault-tolerance methods in extreme-scale systems.This timely monograph has received 85 citations within 4 years, and has become a reference book on the subject.

4 Publication list

Contents

1. Books: 7

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4.1 Books

[1] Patrice Quinton and Yves Robert. *Algorithmes et architectures systoliques.* Etudes et Recherches en Informatique. Masson, 1989. English translation: Systolic algorithms and architectures, Prentice Hall (1991).

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